REMARKS/ARGUMENTS

After entry of this amendment, amending claim 1, 7, 44, and 51, and canceling claims 8 and 9 without prejudice, claims 1-7, 10-15, 44, and 46-54 will remain pending in this application. Support for the amended claims can be found in the specification.

Claims 1-2, 4-5, and 7, and 10-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States patent number 5,479,618 issued to Van de Steeg et al. (hereinafter "Steeg"), in view of United States patent number 4,796,211 issued to Yokouchi et a'. (hereinafter "Yokouchi"). Claims 44, 46-51, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yokouchi in view of Steeg. Claim 52 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yokouchi in view of Steeg, in further view of United States patent number 6,298,360 issued to Muller (hereinafter "Muller"). Claim 54 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yokouchi in view of Steeg, in further view of United States patent number 6,754,830 issued to Laiho et al. (hereinafter "Laiho"). Applicants aver that no new matter has been added in this response.

Claims 1 and 44

Claims 1 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Steeg in view of Yokouchi. But these references do not show or suggest each and every element of claim 1 and claim 44. For example, claim 1 as amended partially recites "loading an initial value in a count register that is a part of a watchdog timer circuit integrated as part of a programmable logic integrated circuit disposed *on a single die*...periodically reloading the count register with the initial value, wherein the reloading is caused by *receiving a first magic value that sets the watchdog timer circuit to respond to a second magic value that is different from the first magic value*, wherein after receiving the first magic value, upon receiving the second magic value, resetting the watchdog timer circuit to the initial value." (emphasis added). Claim 44 as amended partially recites "clocking a watchdog timer circuit on the programmable logic integrated circuit to advance a count register that is a part of the watchdog timer circuit, wherein the programmable logic integrated circuit and the watchdog timer circuit are *disposed on the same die*.. wherein *the first magic value configures the watchdog timer circuit to respond to a*

second magic value that is different from the first magic value". The cited references do not provide this combination of features.

In the Office Action, the Examiner states that Steeg provides each of the recited features with the exception of the watchdog timer operation, and states that Yokouchi discloses the operation of the watchdog timer. In addition, the Examiner states that with regard to claim 44, Muller discloses a final value that is user selectable and that Laiho discloses that in a debug mode the counter does not advance. The Applicants respectfully traverse these rejections.

Steeg discloses a watchdog timer on a first programmable logic circuit 29, and the reloading of configuration data on a second programmable logic circuit 37. The first programmable logic circuit and the second programmable logic circuit are physically and electrically isolated to prevent faults and other noise associated with the second programmable logic circuit from affecting the first programmable logic circuit. As taught by Steeg, without electrical isolation, circuit interruptions and power losses from the second programmable logic circuit (e.g., the I/O circuit) could damage or disable the watchdog timer circuit (e.g., the controller electronics) (See Steeg, Figures 4 and 5, col. 1 lines 32-37, and col. 8, lines 49-59). Therefore, it is not obvious to place the first and second programmable logic circuit on the same die as claimed as Steeg requires physical and electrical isolation.

Yokouchi discloses a watchdog timer employing two counters. The first counter 53 outputs an overflow (carry) signal F when it overflows. The second counter 32 counts the number of times the first counter has been reset. A reset value A is written to latch 31 and compared to the output value B of the second counter via comparator 33. When the reset value and the number of times the first counter match (A=B), the comparator outputs a reset signal C, the first counter is reset via a reset signal E derived from the reset signal C. In order for the resets to continue, a new reset value A, greater in value than the initial reset value A, must be written to latch 31 so that the second counter can continue incrementing before the next reset signal E is asserted. If the next reset value A is not written to latch 31, the first counter 53 overflows and asserts signal F. Yokouchi, Steeg, Muller, and Laiho alone or in combination dc not disclose the watchdog timer circuit and the programmable logic circuit *on the same die.* Even under the assumption that the watchdog timer circuit and the programmable logic circuit

were put on the same die while somehow maintaining electrical and physical isolation, Yokouchi, Steeg, Muller, and Laiho alone or in combination do not disclose *receiving a first magic value that configures the watchdog timer circuit to respond to a second magic value that is different from the first magic value* as claimed. On the contrary, the watchdog timer as disclosed by Yokouchi only asserts the reset signal C when value A initially latched into latch 3 and the value B output of the second counter 32 *are the same value* (e.g., *A=B*) (Emphasis added) (See Yokouchi, Figure 1, col. 4, line 1, through col. 6, line 65).

Applicants submit that neither Muller nor Laiho make up for what Yokouchi and Steeg lack. Therefore, Applicants submit that claim 1 and claim 44 are patentably distinguished over the cited references, alone or in combination.

Claims 1-7, 10-15, and 46-54

Claims 1-7 and 10-15 depend from claim 1, and claims 46-54 depend from claim 44 and are therefore allowable for at least the reasons discussed in relation to claims 1 and 44, as well as the limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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